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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,720	12/02/2003	Roy M. Zeighami	200300353-1	4318

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2835	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,720	ZEIGHAMI ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11 and 16-27* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2006 has been entered.

Election/Restrictions

Newly submitted claims 16-27 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: claims 16-27 are related to Applicant's originally filed (currently canceled) apparatus and system claims as subcombinations disclosed a usable together. Claims 16-27 do not overlap in scope and are not obvious variants, and are separately usable. In the instant case, each of the inventions have utility separable and are distinct from the other subcombinations because the original power supply claims do not require the connection interface to comprise a power selector circuit to comprise a plurality of power selectors arranged in

parallel or the added limitation of a homogeneous power supply module of the invention of claims 16-24.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 16-27 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Foerster (U.S. Pat. No. 3,600,598)

With respect to claim 7 Foerster teaches a method for supplying power to an electronic load (seen in Fig. 2) comprising: connecting a plurality of power supplies in parallel (PS1-PS4); setting, via a power selector circuit (connection of current flow from power supply to load formed with diodes and/or switch means items 28, 32, 34 and 36 see col. 4 lines 19-37 describing the selection or distribution/redistribution of power), a maximum effective voltage for each of said plurality of power supplies to cascade from a highest effective voltage (PS1 +18 volts) for a first (PS1 for example) of said plurality to

a lowest effective voltage (PS 4 -12 volts) for a last (PS4 for example) of said plurality; and interfacing (connection to supply power in Fig. 2) said plurality of power supplies with said electronic load through an said power selector circuit.

With respect to claim 8 Foerster teaches preventing current (see diodes in Fig. 2) generated by one of said plurality of power supplies from sinking into another of said plurality.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foerster (U.S. Pat. No. 3,600,598) in view of Wasaki (U.S. Pub. No. 20030095036) Foerster teaches the process of claim 7, but does not teach the selecting an impedance to create said maximum effective voltage. Wasaki teaches the use of impedance matching circuits (items 20), the matching and selection of impedance values to deliver optimal power or maximum power to an electronic load. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Foerster to include the use of impedance selection to maximize the power output to the load.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foerster (U.S. Pat. No. 3,600,598) in view of Chesavage (U.S. Pat. No. 5,834,925).

With respect to claim 10 Foerster teaches the device of claim 7, however does not teach the limiting said maximum effective voltage of one of said plurality of power supplies to a value of a next one of said plurality when said electronic load causes said maximum effective voltage of said one of said plurality to decrease to said maximum effective voltage of said next one of said plurality. Chesavage teaches a latch circuit (diode) operable to limit the voltage to that of the power unit next to it. The turning on the diode will latch the voltage to that of the supply next to it during power droop. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Foerster to include such a latching to meet load demands.

With respect to claims 11 Chesavage teaches if the voltage of the supply with the higher voltage increases or return from a power droop state the latching component i.e. diode would cutoff deactivating the latching component.

Alternatively Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethellier (U.S Pat. No. 4,760,276) in view of Henze (U.S. Pat. No. 4,924,170)

With respect to claims 7 and 10 Lethellier teaches a method for supplying power to an electronic load comprising (Fig. 2 or 3): connecting a plurality of power supplies (PS1-PS3) in parallel; via a power selector circuit (via opening and closing of item 30), and interfacing said plurality of power supplies with said electronic load through an said power selector circuit. Lethellier further teaches limiting said maximum effective voltage

of one of said plurality of power supplies to a value of a next one of said plurality when said electronic load causes said maximum effective voltage of said one of said plurality to decrease to said maximum effective voltage of said next one of said plurality (see col. 4 lines 9-XX monitoring for a fault or addition of load). The arrangement of Lethellier uses variable resistors (item 20) and power selector (item 30) to equalize the output of the plurality of supplies (col. 3 lines 42-46) until some fault condition in the load or load change occurs (col. 4 lines 10-20) that supply may be isolated so that the problem may be resolved, and loads continue to operate based on the supply level of the adjacent supply (see col. 3 lines 47-53 where Lethellier described N+1 redundancy). Lethellier does not teach the cascading of supplies from highest voltage to lowest voltage as claimed in claim 1. Henze teaches the cascading of a highest effective voltage for a first of said plurality of power supplies to a lowest effective voltage for a last of said plurality of power supplies. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Lethellier in view of Henze to cascade the plurality of supplies in order of effective voltage in order to supply the correct voltage to the load.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Volp (U.S. Pat. No. 4,659,942) teaches a power selector particularly relevant to Applicant's claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

ANATOLY VORTMAN
PRIMARY EXAMINER